REMARKS

Claims 1-8 and 11-14 stand rejected under 35 USC §102(e) as being anticipated by Baras et al., U.S. patent application US 2004/0188138.

Claims 9 and 10 have been withdrawn pursuant to the restriction requirement. Claims 1 and 11 have been amended to more clearly state the invention. Reconsideration and allowance of each of the pending claims 1-8, and 11-14, as amended, is respectfully requested.

Baras et al., U.S. patent application US 2004/0188138 discloses apparatus that substantially reduces or eliminates the resonance that occurs in vias that connect the layers of a printed circuit board by electrically coupling a first transmission line in a circuit board to a second transmission line in a circuit board by two electrical paths having substantially the same electrical length. The two electrical paths are created by connecting the first transmission line to a first via which is in turn connected to a second via having a second transmission line with a plurality of connecting electrical paths between the two vias. In one illustrative embodiment, electrical traces are used to connect the top of the first via to the top of the second via and the bottom of the first via to the bottom of the second via. FIG. 9 shows another illustrative embodiment in accordance with the principles of the present invention whereby two delay lines are used to connect two vias in the same channel in a manner such that the resonance shown in FIG. 4A is substantially eliminated; FIG. 10 shows a plot of the signal loss for the illustrative embodiment of FIG. 9; and FIG. 11 shows a multipin connector in accordance with the principles of the present invention.

Stated at paragraphs 33-40 by Baras et al.:

[0033] While the embodiment of FIG. 7 greatly reduces the negative effects of using a single via for high-frequency applications, and is quite satisfactory for such applications, it tends to require a large footprint on a circuit board. This is because, as discussed above, the signal vias 702A and 702B are separated into different channels by placing a ground via 703 between the two signal vias 702A and 702B. While this electrically isolates the vias from each other, the delay traces 706 and 707 that connect the signal vias must be routed around the ground via at an appropriate distance and, thus, the area of the circuit board required to implement the dual via approach of FIG. 7 is relatively large.

[0034] FIG. 9 shows another illustrative embodiment in accordance with the principles of the present invention whereby dual vias are once again used to eliminate a large portion the signal interference produced by high-frequency use of a single via configuration. However, the embodiment of FIG. 9 takes up much less circuit board space than the embodiment of FIG. 7 because signal vias 902A and 902B are placed in the same channel with no intervening ground via. Thus, the delay traces 904 and 905 do not have to be routed around a ground via and, accordingly, less circuit board space is used.

[0035] In FIG. 9, a signal is introduced onto trace 906 on layer 901A of a circuit board 901 and is conducted in direction 912 on trace 906 toward via 902A. Alternatively, instead of introducing a signal via trace 906, an illustrative connector can be used, such as press-fit connecter 907, to introduce a signal from, for example, an external electronics package. Once again, if a connector is used to introduce a signal into via 902A, trace 906 typically will not be present.

[0036] Once the signal is introduced into via 902A, part of the signal follows path 909 and part of the signal follows path 910. The signal following path 909 is conducted upward along via 902A to delay trace 904 which, in turn conducts the signal to the top of via 902B. The signal is then conducted down via 902B to trace 907. The other portion of the signal entering via 902A is conducted along path 910 down to delay trace 905 and then across to the bottom of via 902B. The signal is then conducted up to signal trace 907 on circuit board layer 901B where it is combined with the signal from path 909 and is routed to a desired destination. Once again, if the electrical length of path 909 is identical to that of path 910, the signals traveling along those paths will combine with no destructive interference.

[0037] FIG. 10 shows a graph of the signal amplitude as a function of frequency that results when the dual via configuration of FIG. 9 is used. The model used to obtain plot 1002 in that figure is identical to that used to obtain plot 403 in FIG. 4B with the exception that each of vias 407 and 411 in FIG. 4B have been replaced with a dual via configuration similar to that shown in FIG. 9, with the vias disposed in a single channel. Referring to FIG. 10 it is evident that the signal loss represented by plot 1002, using a model with the dual vias of FIG. 9, is greatly reduced relative to the single via approach, represented by plot 403. Additionally, plot 1002 also shows increased signal amplitude over plot 802, which represents the signal amplitude of a signal where the signal vias are separated by a ground via.

[0038] One skilled in the art will realize that the embodiment of FIG. 9 represents a model where the signal vias 902A and 902B in that figure are coupled together in a single channel and, thus, experience cross-talk between the two vias. While this cross-talk may produce large resonance between 15 GHz and 20 GHz, depending upon the via and trace configuration, such a single channel arrangement performs well at or above high-frequency levels of approximately 10 Ghz, while requiring a minimum of space on the circuit board.

[0039] The embodiments above have shown how a signal can be either introduced into a via by a signal trace or by a connector, such as a press fit connector. FIG. 11 shows a top view of a portion of a circuit board that represents how the embodiments of the present invention may be used with a typical multipin connector 1101 to attach an external electronics package to a circuit board. In particular, each of vias 1102 (which are vias similar to via 902A in FIG. 9) is electrically connected with two delay lines to a second via 1103, as described in the discussion of FIG. 9. The top delay line 1104 corresponds to delay line 904 in FIG. 9. All of the connectors are disposed within a single channel between ground vias 1106. When a connection is desired each of the pins on a typical multipin connector (e.g., having press fit connection pins), is inserted into vias 1102. In the illustrative embodiment shown in FIG. 11, eight such pins would be inserted into each of vias 1102. The signal from the external package is routed, for example, down via 1102 and the top delay lines 1104 (and the bottom delay line, which is not shown) and is then routed along traces 1105 to a desired destination, as described above.

[0040] The particular configuration of the delay lines and vias when used in the signal-dense environment of a multipin connection, or in other signal-dense environments, must be carefully designed. In particular, the channel size containing the structure of signal vias and ground vias and delay lines shown in FIG. 11 must fit within the typical surface area of a multi-pin connector (e.g., 2 mm.times.2 mm or 2.5 mm.times.1.5 mm). As such, the diameter of the vias and the width and length of the delay lines small enough to maintain the required intrinsic impedance of the via. However, the extremely small vias required to achieve such a required impedance are very often difficult to drill through a typical thick multilayer circuit board. The practical limit of the ratio of via width to board thickness is typically between 1:10 and 1:20 depending on the quality of the board. Therefore, at a typical board thickness of 5.08 mm, the via diameter must stay above 500 microns at a 1:10 ratio. However, this leads to an impedance of about 60 Ohms, which is much lower than the desired 100 Ohm impedance. Therefore, the delay line impedance must be matched accordingly to prevent resonance, in this case to approximately 170 Ohms. However, this is very difficult to achieve with a typical trace line because the trace would be smaller than 100 microns, which is the limit in current printed circuit board lithography.

There are significant differences between what is disclosed in the Baras et al. patent application publication and the pending claims 1-8, and 11-14, as amended;

and the Examiner is respectfully requested to withdraw the rejection of the pending claims 1-8, and 11-14 under 35 U.S.C. §102 because it is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention (Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379, 231 USPQ 81, 90 (Fed. Cir. 1986)). Reconsideration and allowance of each of the pending claims 1-8, and 11-14, as amended, is respectfully requested.

Electronic packages typically include multiple layers or planes including multiple signal, voltage and ground planes. Some electronic packages utilize a mesh structure to construct what appears to be voltage or ground plane. The mesh structure is needed to allow enough non-metal area to insure proper joining or lamination of the plane structures. When designing an electronic package that must utilize a mesh plane, such as, for a power plane or a ground plane, many times the adjacent signal traces may line up with holes in the mesh rather than on the mesh lines. A signal line disposed above or below mesh holes in the mesh plane has a different characteristic impedance than a signal line disposed directly above or below a mesh trace. Signal crosstalk also may occur to a greater extent through the mesh holes to signal traces disposed above or below the mesh holes.

The present invention, as recited in each of the pending independent claims 1 and 11, as amended, provides a method, and computer program product for creating customized mesh planes in electronic packages. The method and computer program product of the present invention is implemented for optimizing signal integrity and to meet all manufacturing limitations for an electronic package.

Each of the pending independent claims 1 and 11, as amended, recite the steps of receiving electronic package physical design data; comparing signal traces in each adjacent plane to a mesh plane with the mesh layout; identifying signal traces in each adjacent plane to the mesh plane adjacent to mesh holes in the mesh layout of the mesh plane; selecting a fill method to replace selected mesh holes with added mesh structure of the mesh plane aligned with the identified signal traces in each adjacent plane to the mesh plane.

Only Applicants teach the steps of identifying signal traces in each adjacent plane to the mesh plane adjacent to mesh holes in the mesh layout of the mesh plane; selecting a fill method to replace selected mesh holes with added mesh structure of the mesh plane aligned with the identified signal traces in each adjacent plane to the mesh plane.

The disclosure of the Baras et al. patent application publication is set forth above in detail, and Applicant respectfully submits that the above limitations, as now expressly recited in independent claims 1, and 11, as amended, are neither disclosed nor suggested by Baras et al. The mesh layout of the mesh plane is different from and are not suggested by signal vias of Baras et al. Each of the independent claims 1, and 11, as amended, is believed to more clearly define the invention and more clearly distinguishes over the disclosure of the Baras et al. patent application publication. Thus, each of the independent claims 1, and 11, as amended, is patentable.

Dependent claims 2-8 and 12-14 respectively depend from patentable claims 1, and 11, further defining the invention. Each of the dependent claims 2-8 and

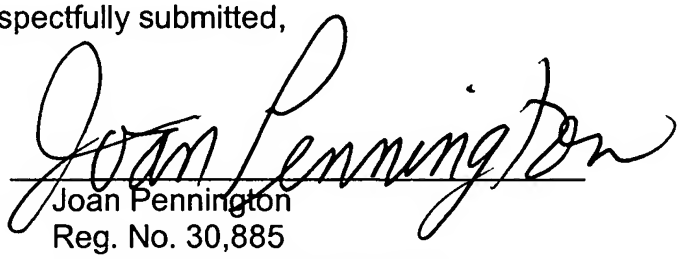
12-14, as amended, is likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-8, and 11-14, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: 

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